UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/757,836 | 01/16/2004 | Craig Hansen | 43876-161 | 5532 |

7590 06/19/2007

McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

| EXAMINER | |
|---|---|
| COLEMAN, ERIC | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 06/19/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/757,836 | HANSEN ET AL. | |
| | Examiner | Art Unit | |
| | Eric Coleman | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☑ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Double Patenting*

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1,4-12,15-22 are provisionally rejected on the ground of nonstatutory double patenting over claims 61,62,69 of copending Application No. 10/436340. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: the claims of the SN 10/436340 and the claims of the instant application are shown side by side below:

| Instant application | SN 10/436340 |
| --- | --- |
| 12.A data processing system comprising (a) a bus coupling components in the data processing system; (b) an external memory coupled to the bus; (c) a programmable microprocessor coupled to the bus and capable of operation independent of another host processor, the microprocessor comprising: a virtual memory addressing unit ; an instruction and data path; an external interface operable to receive data from an external source and communicate the received data over the data path; cache operable to retain data communicated between the external interface and the data path; at least one register file configurable to receive and store data from the data path and to communicate the stored data to the data path; and at least some of the instructions including | 61. A programmable processor comprising an instruction path and a data path; an external interface operable to receive data from an external source and communicate the received data over the data path; a cache operable to retain data communicated between the external interface and the data path; a register file comprising a plurality of registers coupled to the data path; and an execution unit, coupled to the instruction and data paths that is operable to decode and execute instructions received from the instruction path and partition data stored in an operand register in the plurality of registers into multiple operands stored in partitioned fields of the operand register, the execution unit capable of executing group floating point arithmetic |

| Instant application | SN 10/436340 |
| --- | --- |
| A group floating point instruction operating on first and second registers partitioned into a plurality of floating point operands, the floating point operands having a defined precision and the defined precision being dynamically variable, having a defined result precision which is equal to the defined precision of the operands; at least some group floating-point instruction being a group floating point multiply and add instruction, further operating on a third register partitioned into a plurality of floating point operands, the execution unit operable to multiply the plurality of floating point operands in the first and second registers and add the plurality of floating point operands in the third register each producing a floating point value to provide a plurality of floating point values each of the point | operations on floating point data of at least different two precisions in which multiple operands stored in partitioned fields of the operand register are arithmetically operated on to produce a concatenated result that is returned to a register in the plurality of registers, wherein the concatenated result comprises a plurality of individual floating-point results.<br>62. the programmable procesor of claim 61, wherein the execution unit is operable , in response to decoding a single group floating point add instruction specifying (i) a precision of a group operation corresponding to an elemental width of m-bits of operands |

Instant application

values capable of being represented by the defined result precision, and a concatenated result having a plurality of partitioned fields for receiving the plurality of floating point values.

SN 10/436340

(ii) an address of a first register in the register file having a width of n-bits and holding n/m floating point operands in partitioned fields, and (iii) an address of a second register in the register file having width of n-bits an holding n/m floating point operands in portioned fields, to add each operand stored in a portioned field of the first register with a corresponding operand stored in a partitioned field of the second register to produce n/m floating point results that are returned as concatenated result are partitioned fields of a register in a plurality of registers.

69. the programmable processor of claim 62 wherein the execution unit is further operable in response to decoding a single group floating point multiply-add instruction specifying a precision...

As can be seen from the side by side showing of the representative independent claim 12 of the instant application along the claim 61 and dependent claims 62 an a portion of dependent claim 69 of SN 10/436340 the claims of both the instant application an SN 10/436340 are substantially similar . As to the differences, since the Since SN 10/436340 in claim 61 above comprised a external interface and storing data received from external interface it would have been obvious to one of ordinary skill that in at least one implementation the external data was from an external memory coupled to a bus. Also one of ordinary skill would have implemented the processor of 10/436340 as a microprocessor to take advantage of the reduced cost and reduced size implementing the invention as microprocessor. As to the virtual addressing unit this unit does not perform any claimed operation. Therefore since the use of a virtual addressing unit in a DP system for facilitating addressing plural groups of registers or memory locations where virtual addresses facilitates simplifying addressing of locations in a program then one of ordinary skill would have been motivated to use a virtual address unit in the 10/436340 system.

Claim 1 of the instant case has similar limitations to claim 12 however claim 1 comprising limitations to floating point multiply and add operations where data from plural registers are multiplied and data from another single register are added and the concatenation of results. These limitations are part of claim 69 in 10/436340.

As to the limitations of claims 4,6-11 and 15,17-22 of the instant application , the specifications of the fields would have been obvious in view of the IEEE 754 standard floating point format.

As per claims 5,16, of the instant application, 10/436340 comprises the concatenated results stored in a register in claim 62.

Claims 2,3,13,14 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 61,62,69 of copending Application No. 10/436,340 in view of Kohn (patent No. 5,081,698.

As to the limitation of set less than and set greater than Kohn taught this type of comparison operation determining the smaller of two values in a system that perform partitioned arithmetic (e.g. see figs. 1,2,3a,3b, and col. 5, lines 6-67). With the less than comparison the use of the greater than comparison would have been within the level of skill of one of ordinary skill the art implementing the claimed system and the Kohn teachings. Further Kohn taught a mask that characteristically comprises a zero value an identity value for selecting data to read the result (e.g. see fig. 4 and col. 6, lines 40-64 of Kohn).

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

This is a provisional obviousness-type double patenting rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

ERIC COLEMAN
PRIMARY EXAMINER